Elisa VIANELLO, born February 21, 1981
Nationality: Italian/French
https://scholar.google.com/citations?user=hscO0hMAAAAJ&hl=it

- **EDUCATION**

2010 **PhD** double degree from the University of Udine (Italy), and National Polytechnical Institute of Grenoble (INPG – CEA Leti, France). Supervisors: prof. Luca Selmi and Dr. Gerard Ghibaudo.

2006 **M. Sc.** degree in Electrical Engineering with first class honours (University of Udine, Italy).

- **CURRENT POSITION**

2022-2027 **ERC Consolidator Grant DIVERSE** on "Heterogeneous integration of imprecise memory devices to enable learning from a very small volume of noisy data".

2020 –now **Edge Artificial Intelligence Program Coordinator**, at CEA Leti (Grenoble, France)
I oversee a program pioneering hardware-level solutions to create energy efficient and reliable Edge AI solutions. The program involves over 30 researchers. I directly supervise 3 PhD students.

2020–2022 **Coordinator of the "MeM-Scales" (2020-2022) European project (H2020)** focused on the co-development of a novel class of algorithms, devices and circuits that reproduce multi-timescale processing of biological neural systems.

2015 – now **Senior scientist** at CEA Leti (Grenoble, France)
I conduct research activities in the field of bio-inspired circuits for AI applications, combining resistive memory technologies, information coding and learning strategies.

- **PREVIOUS POSITIONS**

2011 – 2015 **Junior scientist** at CEA Leti (Grenoble, France)
I conducted research activities in the field of modelling and characterization of resistive memories (CBRAM with Altis; OxRAM with STMicroelectronics).

2010 – 2011 **Postdoctoral researcher** at Fondazione Bruno Kessler (Trento, Italy)
I developed Silicon Radiation Detectors for the Large Hadron Collider at CERN (Genève).

- **INSTITUTIONAL RESPONSIBILITIES**

2023 – now **Member of the Technical Program Committee** of the IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)

2019 – now **Chairman of the memory devices and circuits towards non Von Neumann track** in the European Solid State Device Conference (ESSDERC).

2020 – 2021 **Member of the Technical Program Committee** of Electron Devices Technology and Manufacturing (EDTM), Subcommittee Member for Memory.

2016 – 2017 **Member of the Technical Program Committee** of the Internal Electron Device Meeting (IEDM), Subcommittee Member for Circuit Device Interaction.

2015 – 2019 **Member of the Technical Program Committee** of European Solid State Device Conference (ESSDERC), Subcommittee Member for Memory Technology.

2015 – 2020 **Member of the NanoGiga Technical Committee,** International Symposium on Circuit and Systems (ISCAS).

2013 – 2014 **Member of the Technical Program Committee** of the International Reliability Physics Symposium (IRPS), Subcommittee Member for Memory Technology.

- **REVIEWING ACTIVITIES**

Editorial commitments: member of the editorial board of the *Neuromorphic Computing and Engineering* IOP Science journal (2019-now); associate editor of the *Special issue on Emerging Materials in Neuromorphic Computing,* AIP APL Material (2020); associate editor of the IEEE Trans. on Circuits and Systems –II (2020-2021)

Reviewing commitments: *IEEE Transaction of Electron Devices, Electron Devices Letter, Transaction On Nanotechnology, Transactions on Very Large Scale Integration, Transactions on Circuit and Systems, Solid State Electronics, Microelectronic Reliability* (2009-now)*; Nature, Nature Electronics, Nature Machine Intelligence and Nature Communications* Journals (2019-now).

- **MEMBERSHIPS IN SCIENTIFIC SOCIETIES**

2011 –now **Member** of the Institute of Electrical and Electronics Engineer (IEEE)

- **Ten Selected Publications**

I have been team leader in charge of the development of new applications for resistive memory technologies at CEA-Leti for the past 10 years. The following publications illustrate achievements beyond the state-of-the-art in the field of brain inspired computing and In-Memory Computing.

- T. Dalgaty, N. Castellani, C. Turck, K.-E. Harabi, D. Querlioz, and **E. Vianello**, "In situ learning using intrinsic memristor variability via Markov chain Monte Carlo sampling", *Nature Electronics***,** vol. 4, pp. 151–161, January 2021.
- F. Moro, E. Hardy, B. Fain, T. Dalgaty, P. Clémencon, A. De Prà, E. Esmanhotto, N. Castellani, F. Blard, F. Gardien, T. Masquida, F. Rummens, D. Esseni, J. Casas, G. Indiveri, M. Payvand, **E. Vianello**, "Neuromorphic object localization using resistive memories and ultrasonic transducers", *Nature communications,* vol.13, June 2022.
- E. Esmanhotto, L. Brunet, N. Castellani, D. Bonnet, T. Dalgaty, L. Grenouillet, D. R. B. Ly, C. Cagli, C. Vizioz, N. Allouti, F. Laulagnet, O. Gully, N. Bernard-Henriques, M. Bocquet, G. Molas, P. Vivet, D. Querlioz, J.M. Portal, S. Mitra, F. Andrieu, C. Fenouillet-Beranger, E. Nowak and **E. Vianello**, "High-Density 3D Monolithically Integrated Multiple 1T1R Multi-Level-Cell for Neural Networks", International Electron Device Meeting (IEDM), 2020.
- D. R. B. Ly, J-P. Noel, B. Giraud, P. Royer, E. Esmanhotto, N. Castellani, T. Dalgaty, J-F. Nodin, C. Fenouillet-Beranger, E. Nowak and **E. Vianello**, "Novel 1T2R1T RRAM-based Ternary Content Addressable Memory for Large Scale Pattern Recognition", IEEE International Electron Devices Meeting (IEDM), 2019.
- A. Valentian, F. Rummens, **E. Vianello**, T. Mesquida, C. Lecat-Mathieu de Boissac, O. Bichler, C. Reita, "Fully Integrated Spiking Neural Network with Analog Neurons and RRAM Synapses", IEEE International Electron Devices Meeting (IEDM), 2019.
- D. R. B. Ly, A. Grossi, C. Fenouillet-Beranger, E. Nowak, D. Querlioz, **E. Vianello**, "Role of synaptic variability in resistive memory-based spiking neural networks with unsupervised learning", *Journal of Physics D: Applied Physics*, vol. 51, no. 44, August 2018.
- **E. Vianello**, T. Werner, O. Bichler, A. Valentian, G. Molas, B. Yvert, B. De Salvo, L. Perniola, "Resistive memories for spike-based neuromorphic circuits", IEEE International Memory Workshop (IMW) 2017 (Invited).
- D. Garbin, **E. Vianello**, O. Bichler, Q. Rafhay, C. Gamrat, G. Ghibaudo, B. DeSalvo, L. Perniola, "HfO_2-Based OxRAM Devices as Synapses for Convolutional Neural Networks", IEEE Transactions on Electron Devices vol. 62, no. 8, pp 2402-2409, August 2015.
- **E. Vianello**, O. Thomas, G. Molas, O. Turkyilmaz, N. Jovanovi, D. Garbin, G. Palma, M. Alayan, C. Nguyen, J. Coignus, B. Giraud, T. Benoist, M. Reyboz, A. Toffoli, C. Charpin, F. Clermidy, L. Perniola, "Resistive Memories for Ultra-Low-Power embedded computing design", International Electron Device Meeting IEDM, 2014.
- M. Suri, D. Querlioz, O. Bichler, G. Palma, **E. Vianello**, D. Vuillaume, C. Gamrat, B. De Salvo "Bio-inspired stochastic computing using binary CBRAM synapses", IEEE Transactions on Electron Devices, vol. 60, no. 7, pp 2402-2409, July 2013.

- **INVITED PRESENTATIONS**

20 invited talks, 12 at international conferences and 8 at international advanced schools including:

- Tutorial talk at Electron Device Meeting, IEDM, 2022 (San Francisco).
- Tutorial talk at International Memory Workshop, IMW, 2021 (Dresden).
- Keynote presentation at IEEE Smart Systems Integration 2021 (Grenoble).
- Tutorial talk at International Conference on IC Design and Technology 2019.