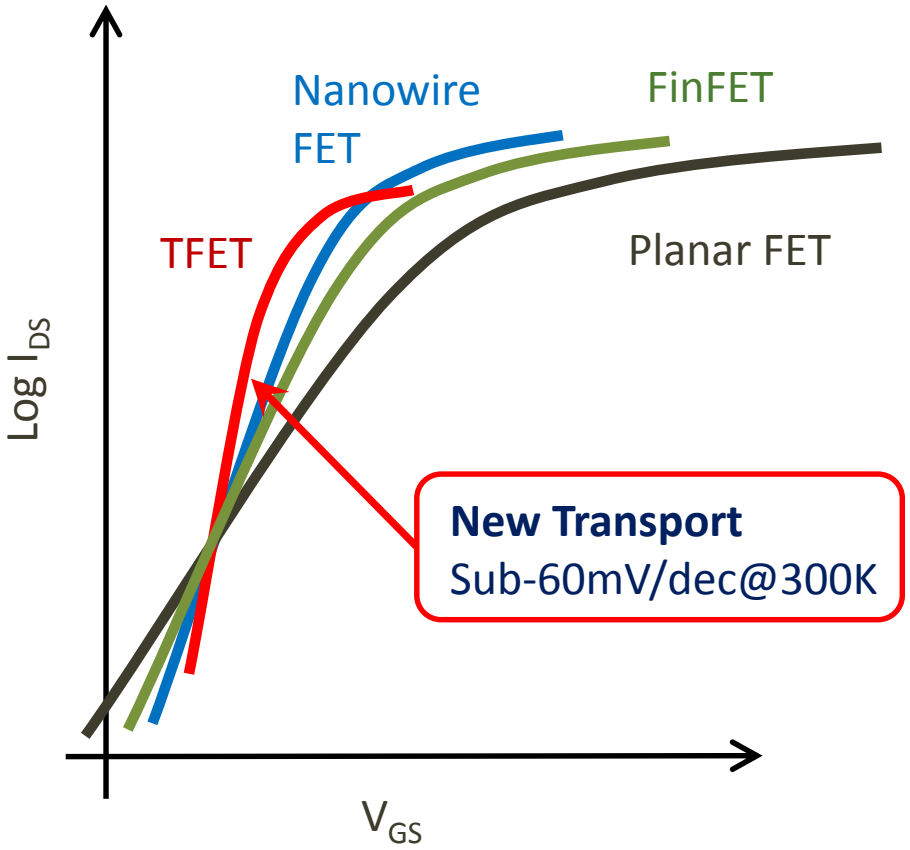
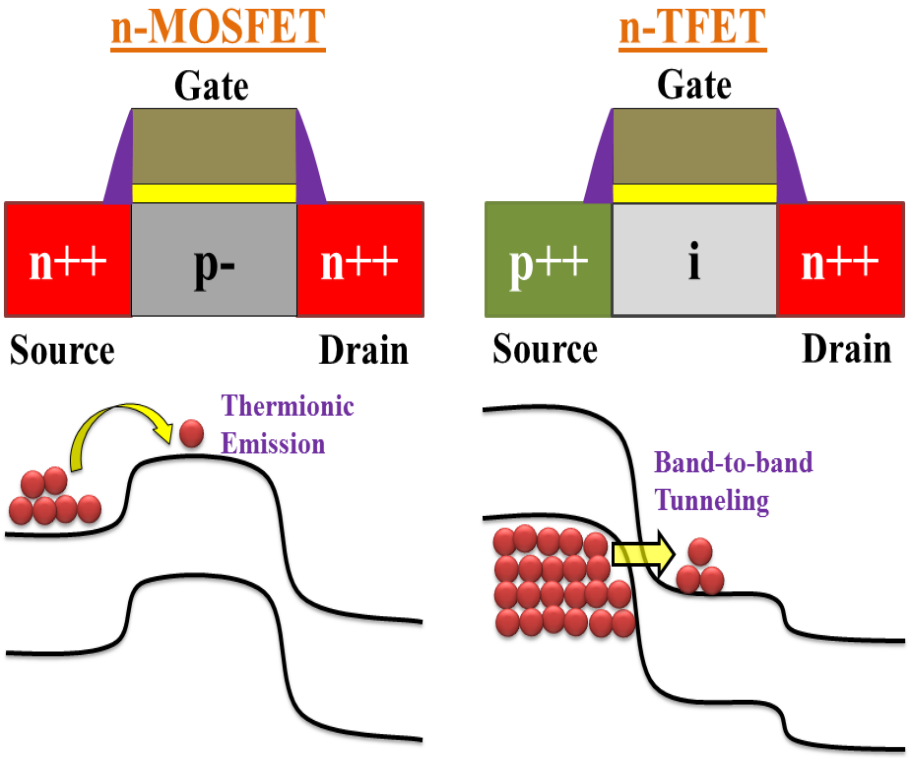
Forth IU.NET Day
21 September, 2017 – Perugia

Perspectives of Tunnel FETs as energy-efficient electronic switches

E. Gnani

Tunnel FET: device concept



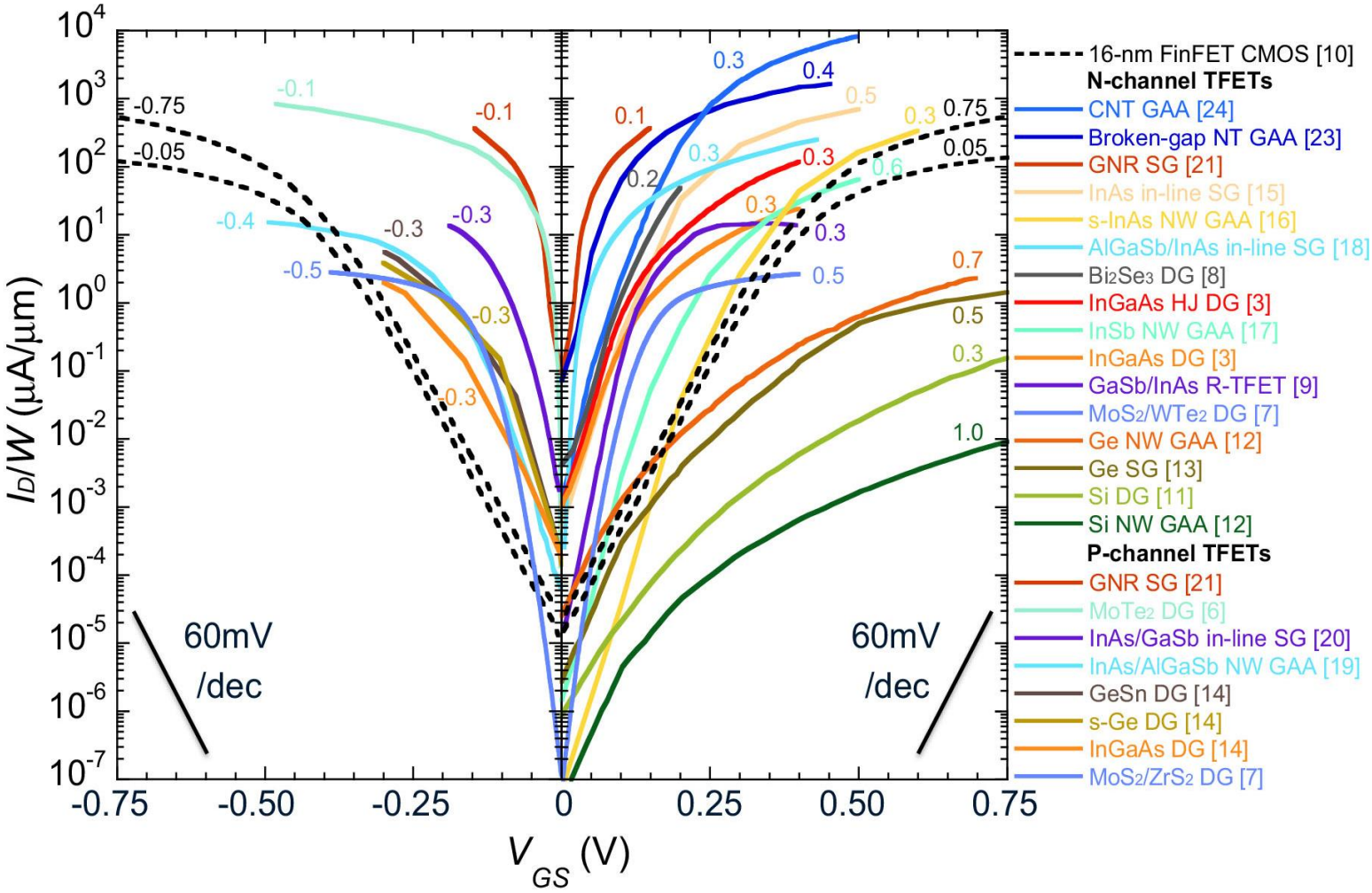


filtering high energies out

E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

TFET: theory vs. reality

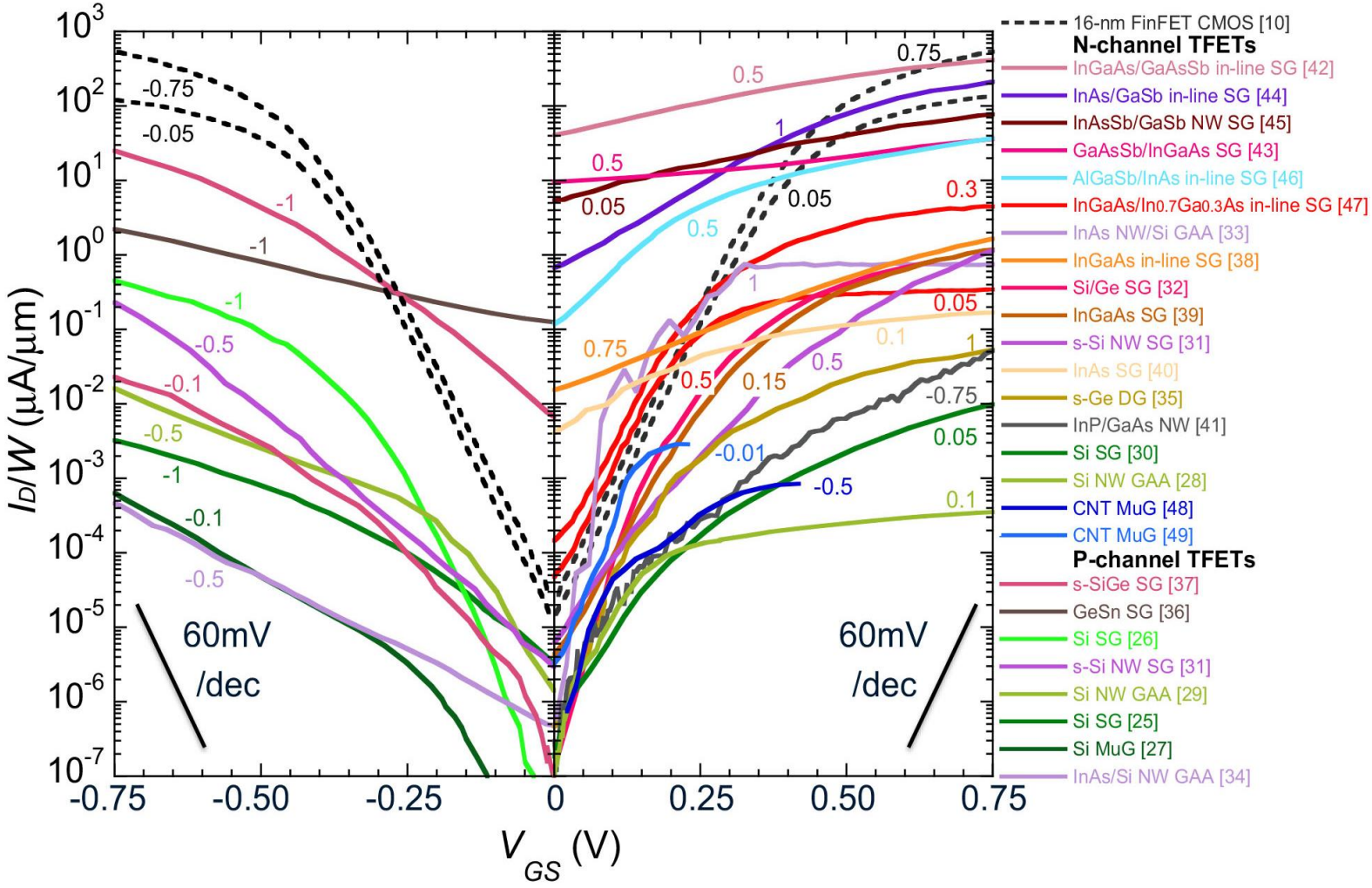
Simulations



H. Lu and A. Seabaugh, J. of the EDS, 2014

TFET: theory vs. reality

Measurements



H. Lu and A. Seabaugh, J. of the EDS, 2014

TFET potential strengths/limitations

TFET Strengths

- Very effective filtering of high-energy electrons
- Nearly ideal saturation of the TFET output characteristics
- Good thermal stability

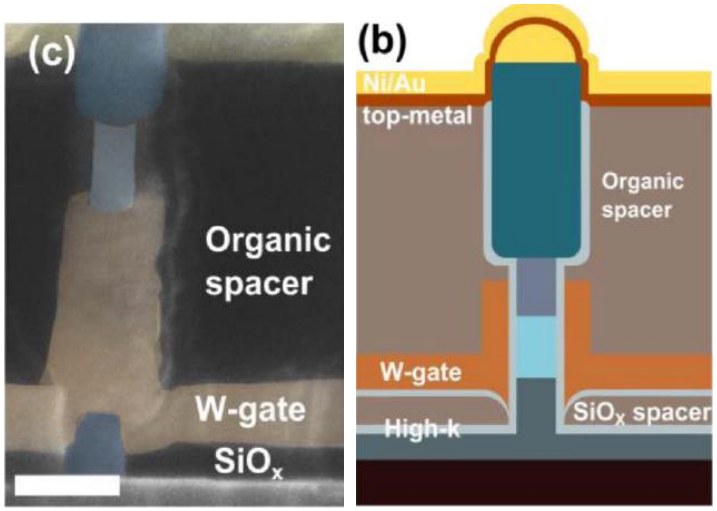
TFET Limitations

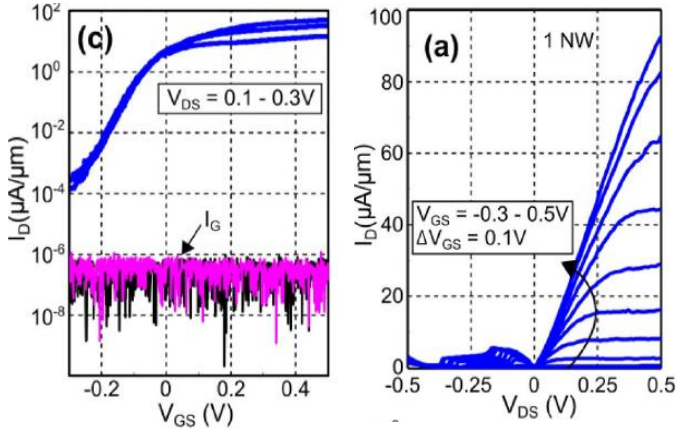
- Small I_{ON} (tunneling)
- Ambipolarity and Unidirectionality (no pass transistor)
- Small SS extended over a limited range of currents
- trap-assisted tunneling/defects at the S/CH junction
- Small drain conductance at low V_{ds}
- Strong sensitivity of the onset voltage with device size;
- Large C_{GD}

TFET: best experimental realizations

InAs/InGaAsSb/GaSb NW TFET

Memisevic et al., TED, 2017

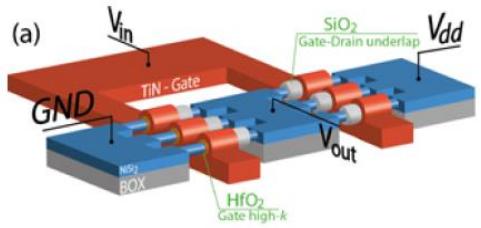


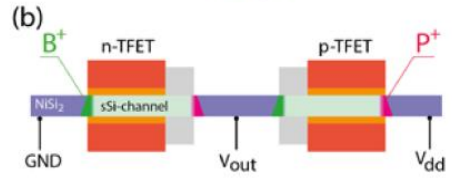


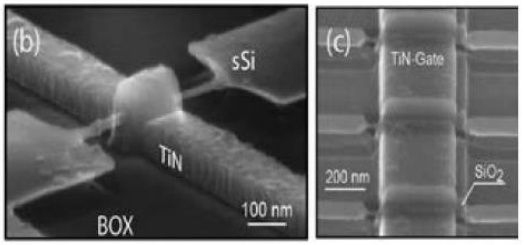
SS= 43 mV/decade @ V_{DS} = 0.1 V

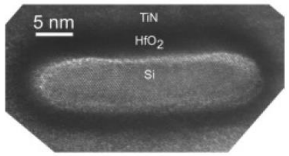
Silicon GAA NW TFET Inverter

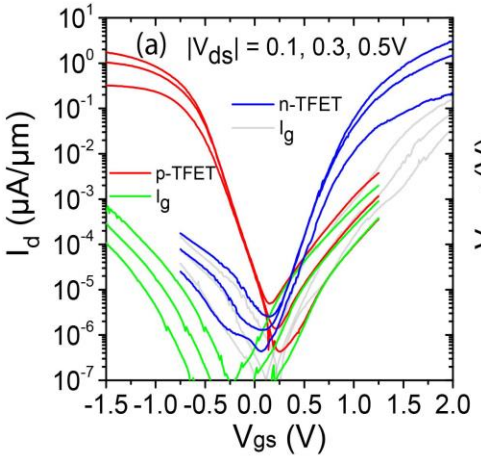
G. V. Luong et al., EDL, 2016

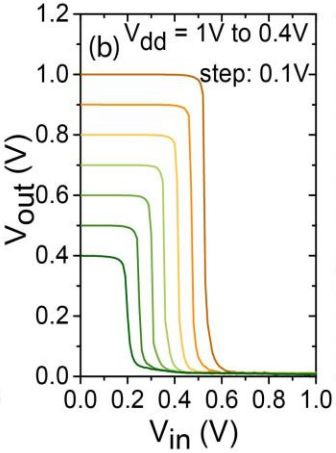


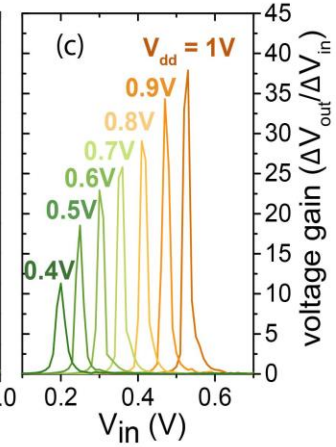






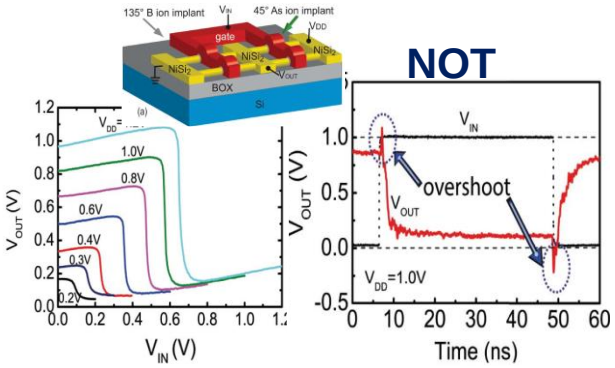






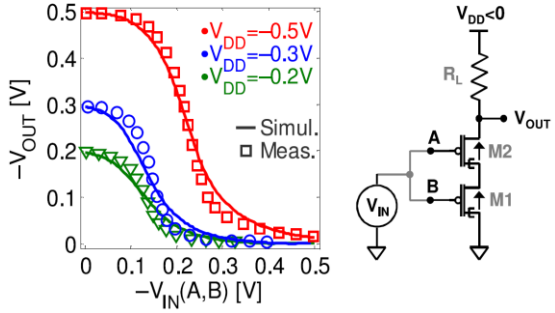
TFET applications

Digital

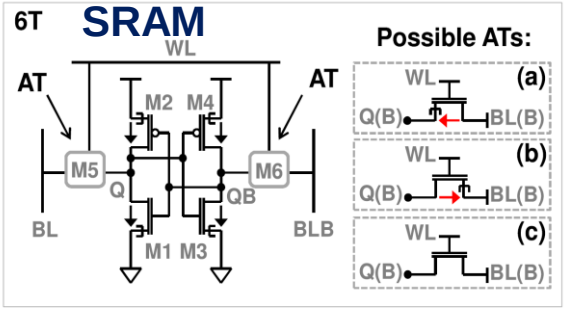


L. Knoll et al., EDL, 2013

NAND

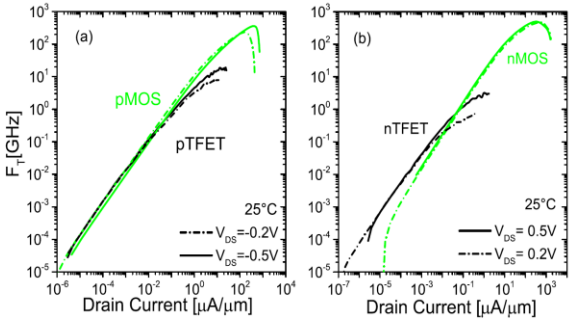


SRAM



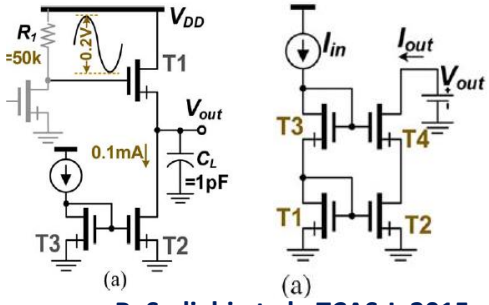
Strangio et al., JEDS, 2015

Analog



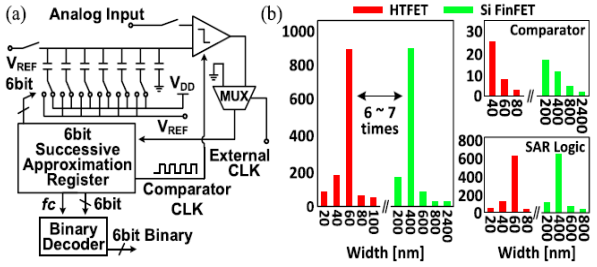
A. Biswas et al., TED, 2017

Sorce follower&current mirror



B. Sedighi et al., TCAS-I, 2015

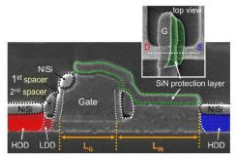
ADC converter

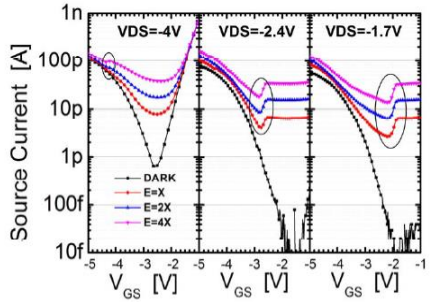


M.S. Kim et al., TED, 2014

Sensors

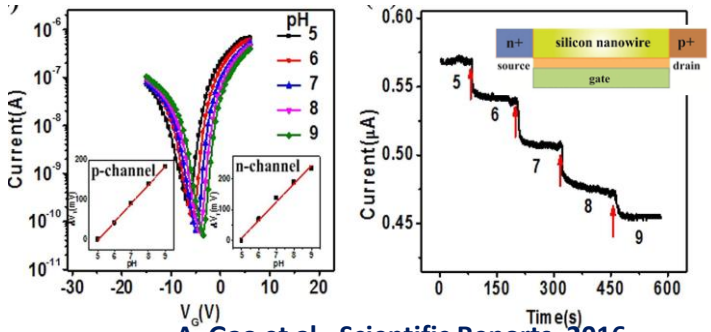
Optical sensing





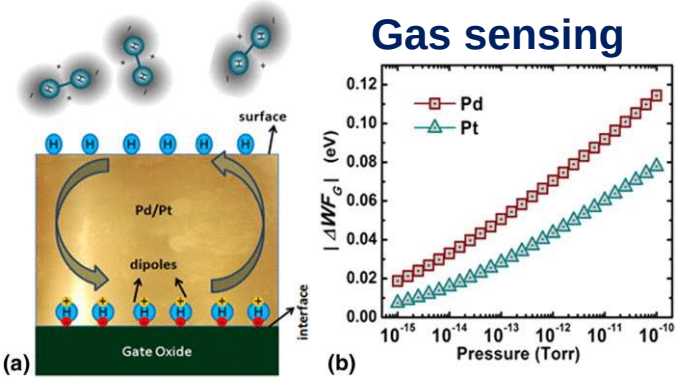
N. Dağtekin et al., ESSDERC, 2014

PH sensing



A. Gao et al., Scientific Reports, 2016

Gas sensing



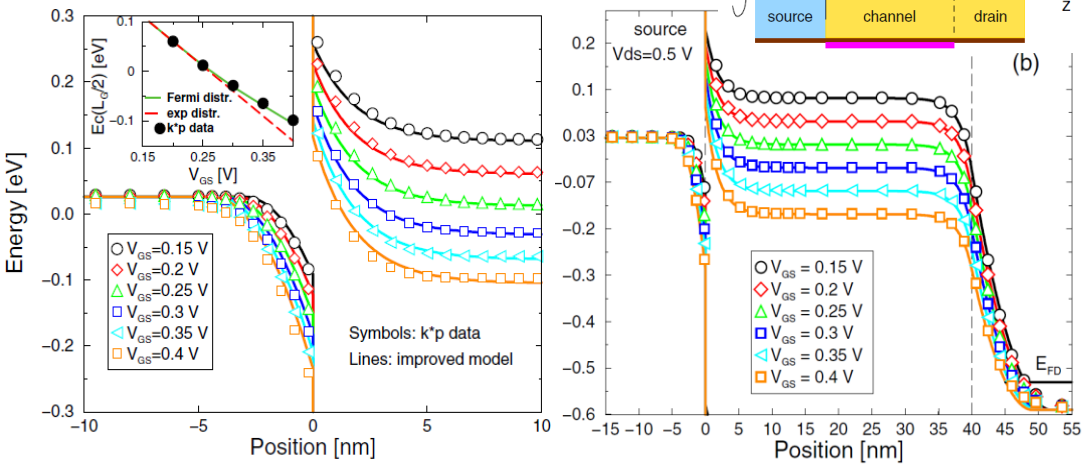
D. Sarkar et al., APL, 2013

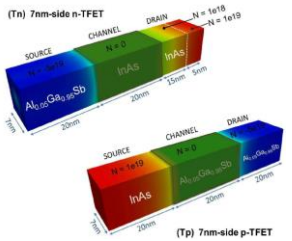
IU.NET Capabilities

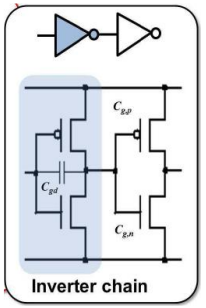
- Device simulation:
  - ✓ semiclassical (DD, Monte Carlo, with tunneling as an additional G/R rate)
  - ✓ quantum mechanical (non-parabolic EM, full quantum **k*p**).
- Modeling of non idealities: TAT, interface traps, strain.
- Evaluation of performance degradation due to electrical stress.
- Performance estimation of analog and digital TFET circuits (Verilog-A)

E2Switch project

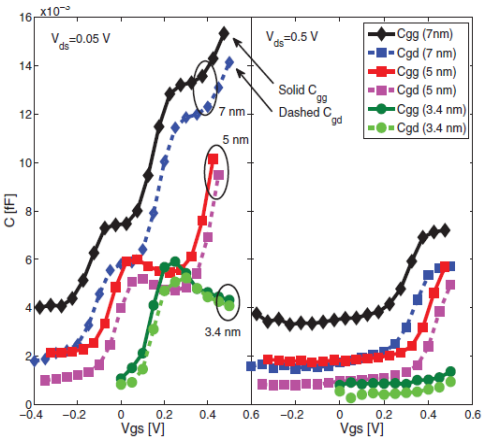
compact models



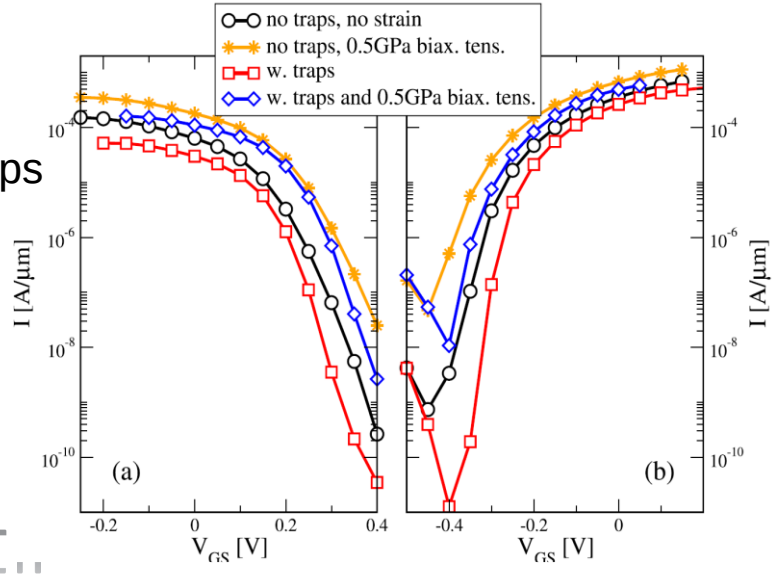


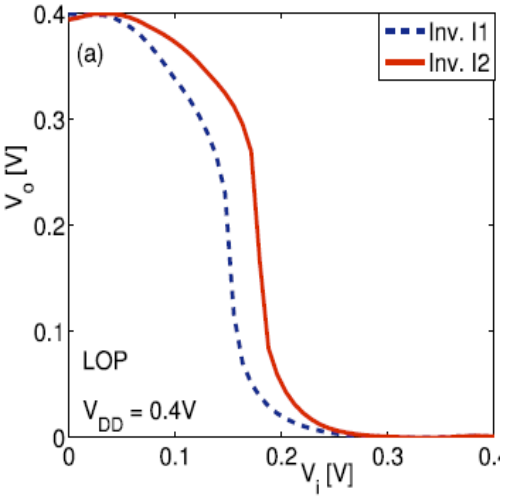


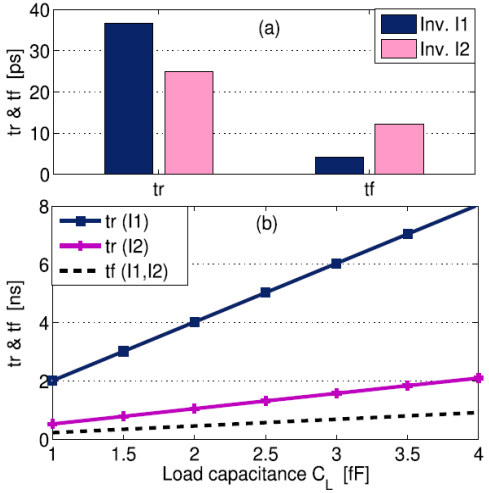
AlGaSb/InAs technology platform



interface traps and strain





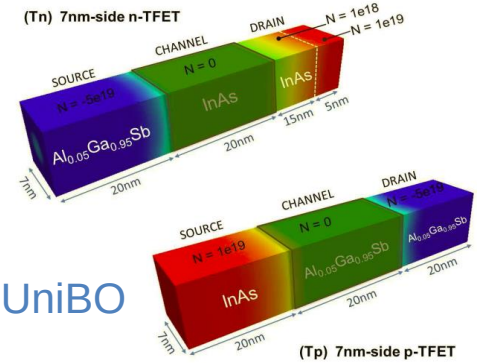


E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

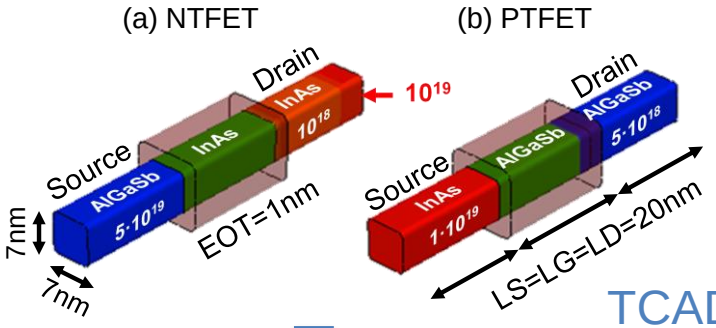
Evaluation of TFET circuits: methodology

- Collaboration between UniBO, UniUD and UniCAL.

E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits



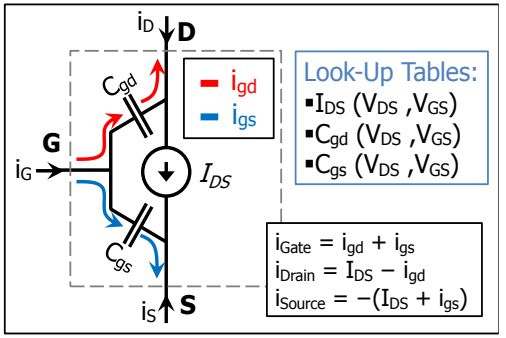
NEGF from UniBO



TCAD templates

Circuit simulations

Cadence Virtuoso environment

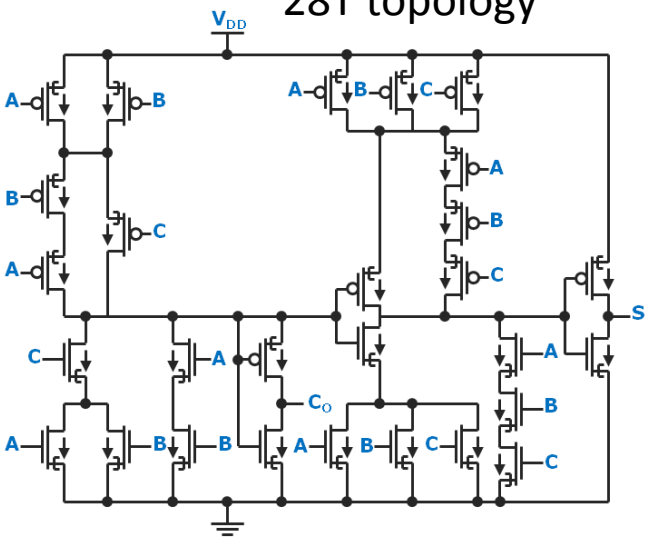


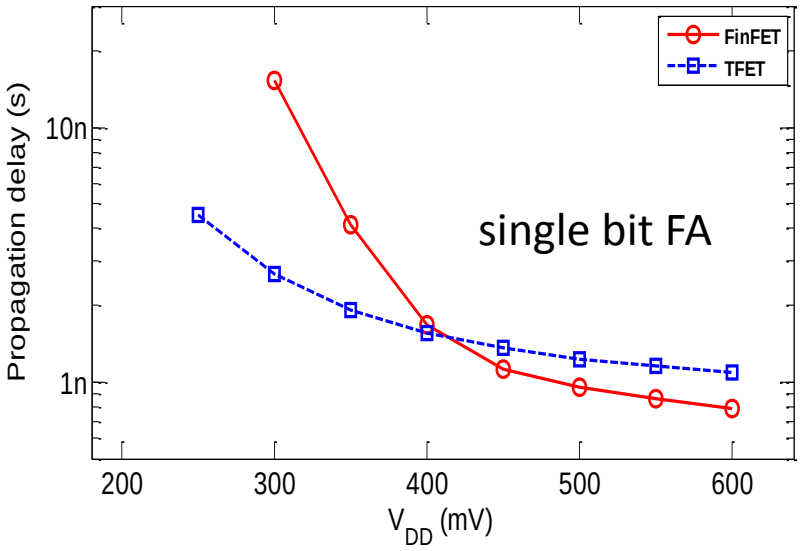
Look-up-tables in Verilog-A

- methodology applied to SRAM cells, full-adders, level-shifters, comparators, track-and-hold, op-amps.

Evaluation of TFET circuits: Full-Adder

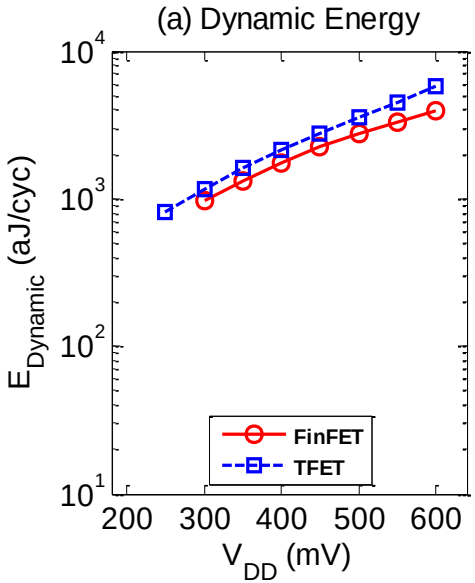
28T topology

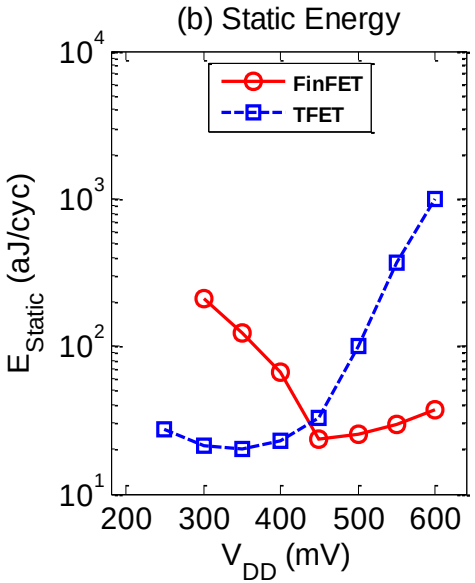




TFETs faster than FinFETs for V_{DD}<0.4V

32bit ripple carry adder



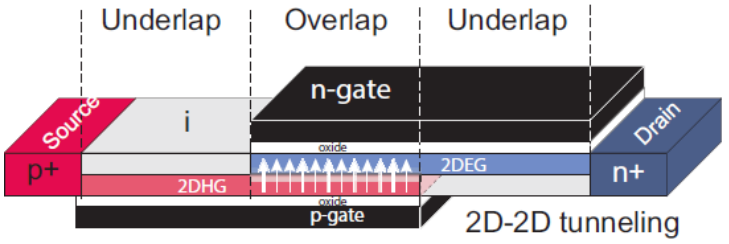


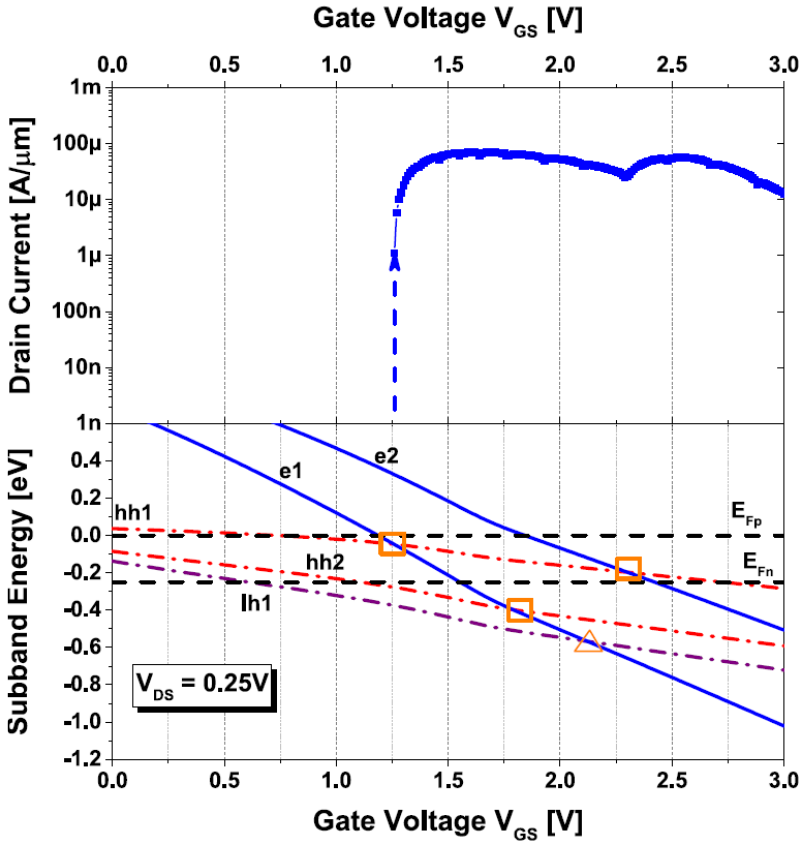
similar dynamic energy but lower static energy at low V_{DD}

E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

Alternative geometries

- Modeling the electron-hole-bilayer-TFET (UniUD+EPFL)

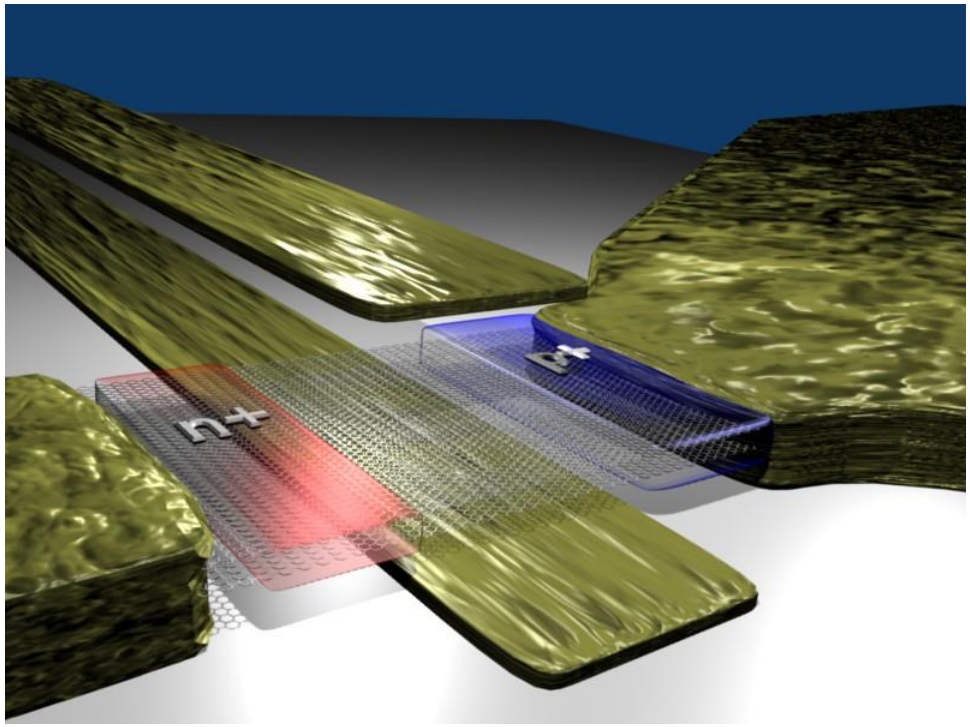


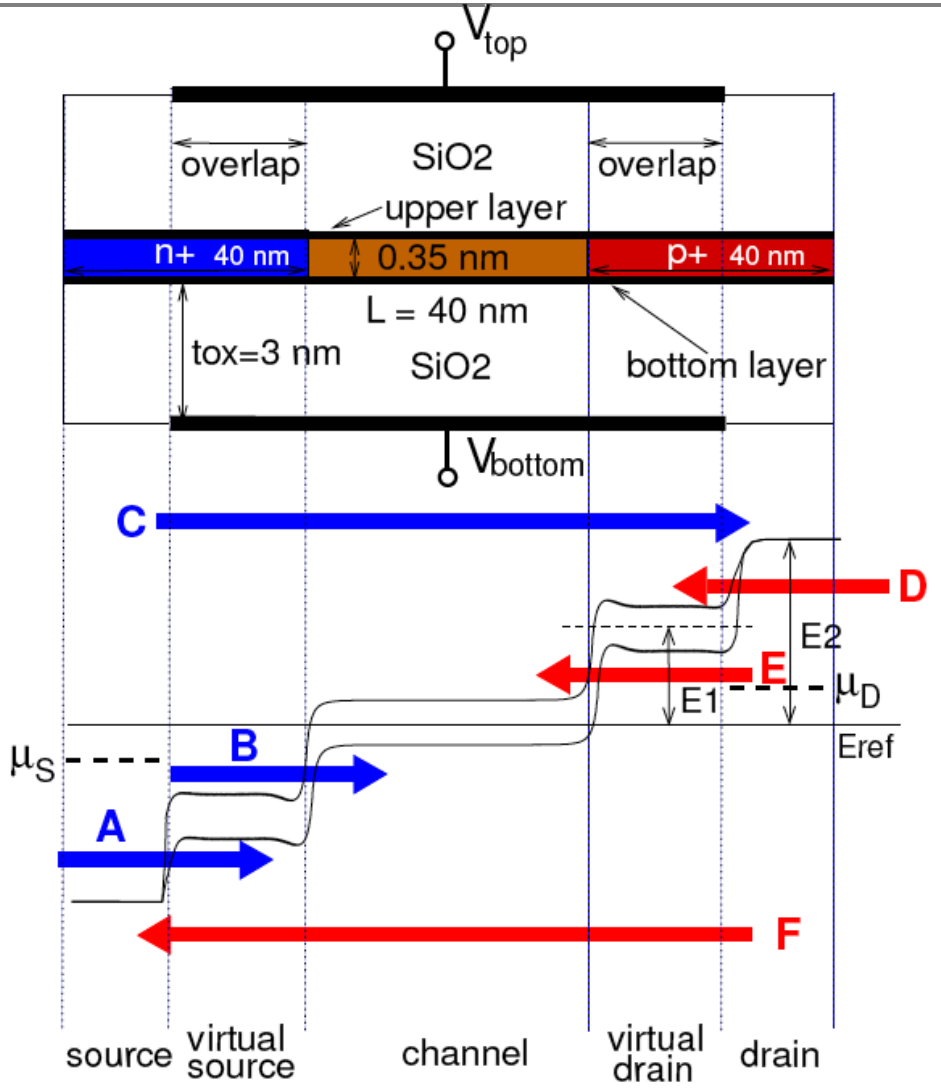


- BTBT between el. and ho. inversion layers
- current steps when subbands align
- non-self-consistent full-quantum model
- verified against NEFG from UniBO

E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

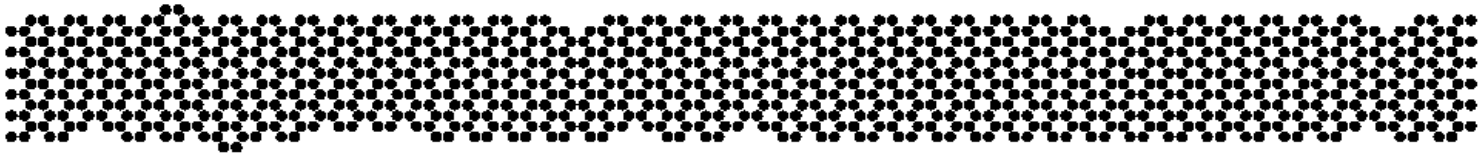
Tunnel FET Bilayer graphene FET





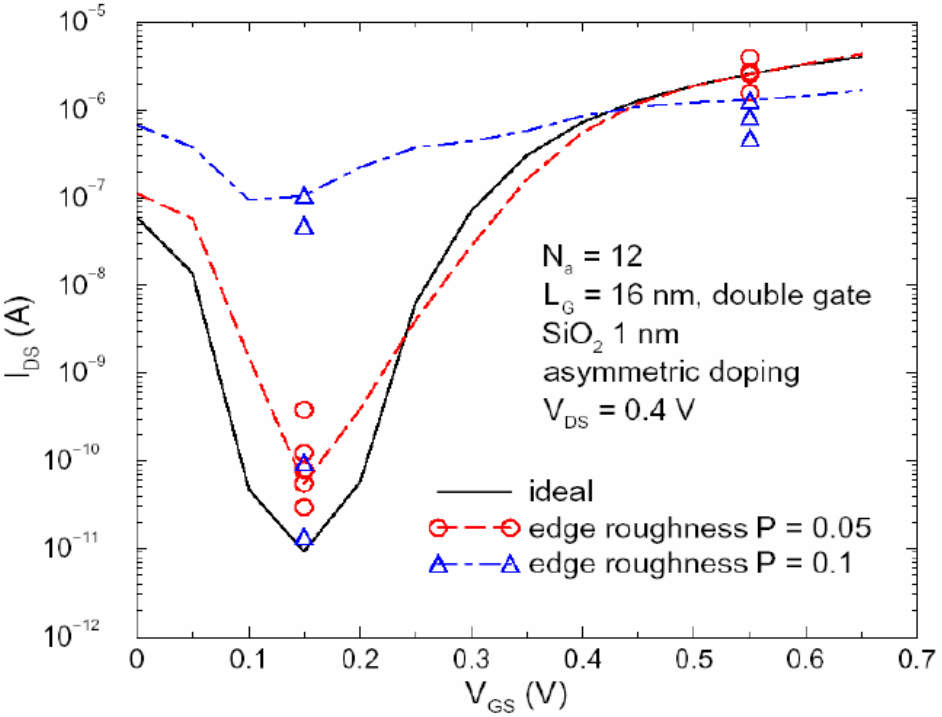
- UniPI has explored the possibility of BG in TFETs.
- No EBL restrictions as in GNRs.
- Proper band engineering to reduce tunneling current in the OFF state.

Tunneling GNR FET: effect of edge roughness

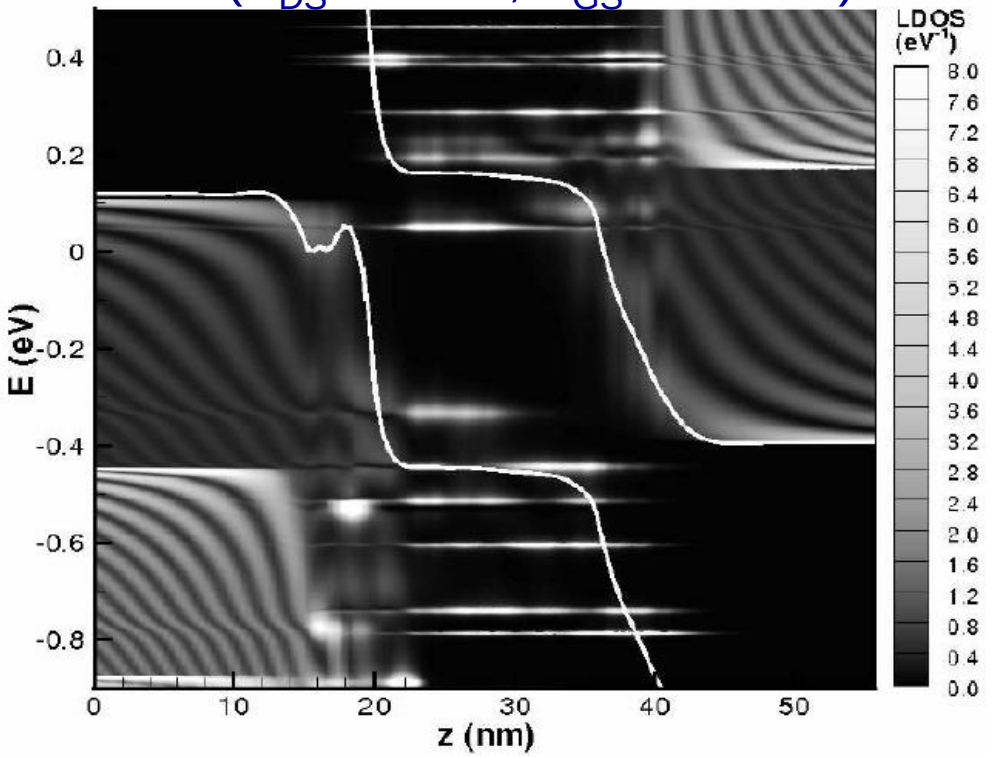


Typical N_a = 12 channel with edge roughness probability P = 0.1

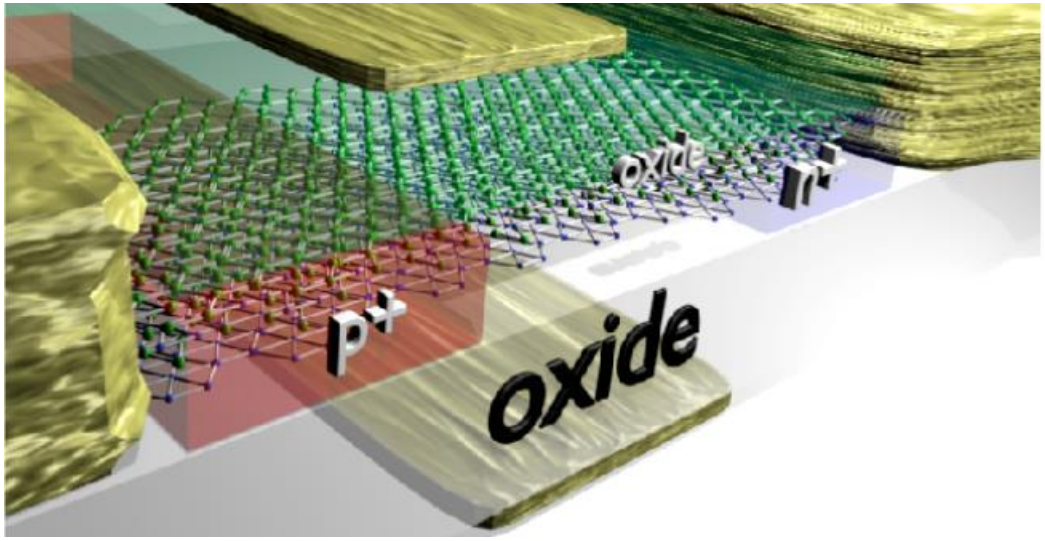
Only a mild roughness can be tolerated !!

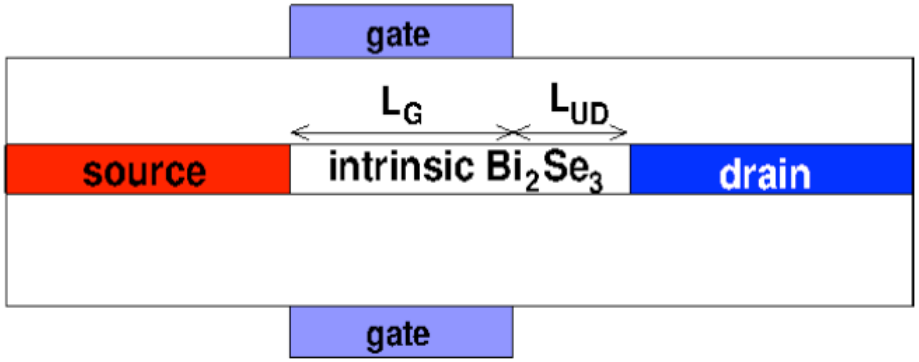


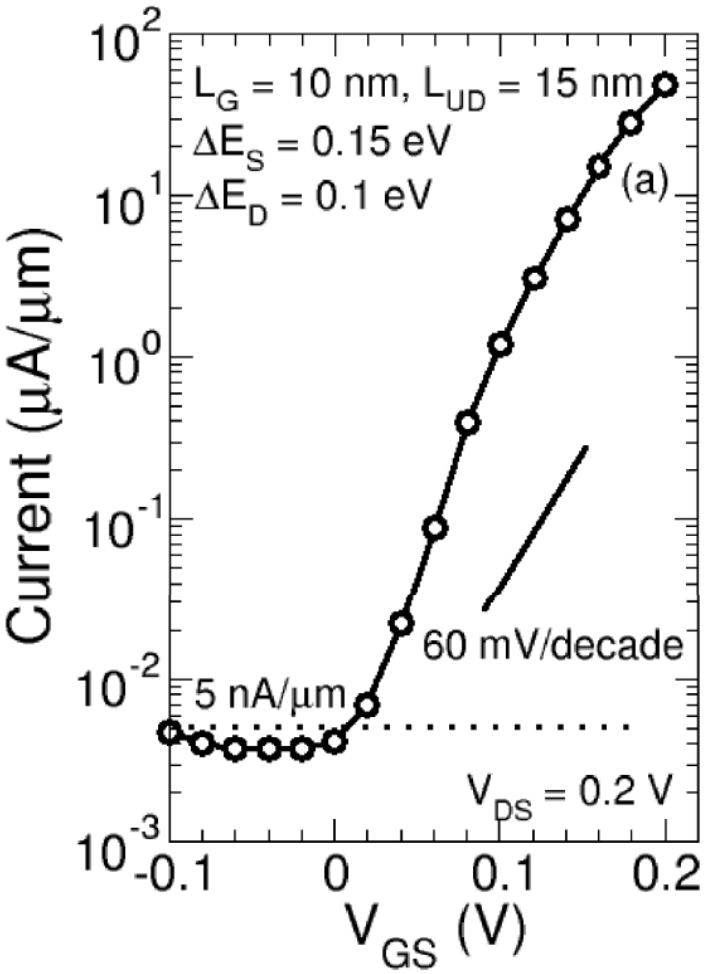
Local density of states (V_{DS} = 0.4 V, V_{GS} = 0.15 V)



Bi_2Se_3 T-FET







[Q. Zhang, G. Iannaccone, G. Fiori "Two-dimensional tunnel transistors based on Bi2Se3 Thin Film", IEEE Electr. Dev. Lett., Vol. 35, p. 129, 2014]

Future developements

- Calibration of TFET models with different complexity.
- Performance estimation and benchmark of circuits for analog&digital applications.
- Know-how on modeling of TFETs can be exploited also for heterogeneous CMOS/TFET circuits.
- TFETs in 2-D Transition Metal Dichalcogenide Materials