LFOUNDRY Solutions for great visions | A SMIC COMPANY

Evolution of an Italian Semiconductor Fab: Opportunities and Perspectives

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LFOUNDRY A SMIC COMPANY

Outline

- **The Avezzano Fab**
- The Technology Opportunities
- The Development Perspective

The Avezzano Fab at a Glance

Key Facts

- Located in Avezzano, (L'Aquila), Italy
- Founded: May, 1989
- 8" capacity of 40.000 wafer/month
- ~200M€ turnover in 2016
- ~1500 employees

The Avezzano Fab History

IDM* model

- 1989 - 6 inch, DRAM, Texas Instruments
- 1994 - 8 inch mini line DRAM
- 1998 - acquired by Micron Technology
- 2001 - complete 8 inch conversion
- 2004 - record efficiency and stability
- 2005 - image sensor line installation
- 2006 - CMOS Imager Sensors (CIS) development and production
- 2008 - creation of Aptina Imaging → 1st foundry customer

Foundry model

- 2013 - leveraged buy out to a joint venture between LFoundry Europe Gmbh (German entity) and Marsica Innovation spa. (Italian entity)
- 2014 - reorganization to new LFoundry srl
- 2016 - acquisition of 70% of the shares by SMIC from the two German and Italian owners

* IDM = Integrated Device Manufacturer

Technology at a Glance

	Key Feature
Avezzano Fab Capability	65nm Smallest Litho Feature 90nm Volume Production Al and Cu Metallization
Basic FOT CMOS Platform	Technology Nodes: 150nm 110nm
Technology Specialization	Optical Sensors (CIS, Discrete PD, SiPM) Analog and Mixed Signal Smart Power (LDMOS)
Special Modules	Back-side Process Wafer Thinning and Stacking Lithographic Stitching

5

Engagements Models

Innovative in technology, partnership- and supply- models in secure environment

- Mainstream technology with modules
- PDK platforms
- Specific qualifications for automotive and security

Open Foundry
design environment and wafer fabrication

- Special know how and capabilities in imaging technology
- Volume aluminum and copper metallization
- Engineering know how for CMOS technology

Customer Technology
adopting customer technology

- Wide network to research center and leading universities in Europe

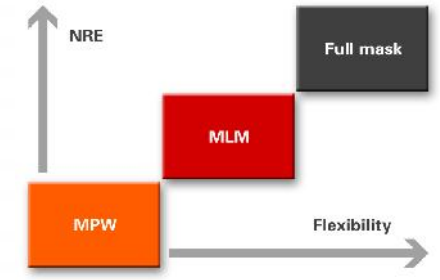
Joint Technology Development
technology development and production partnership

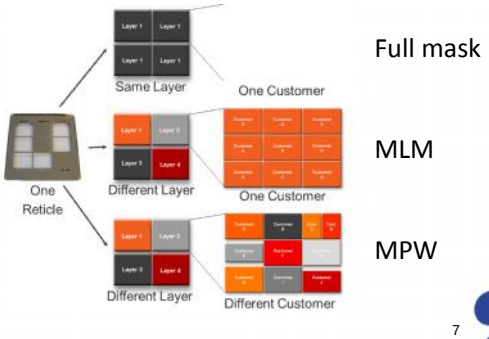
6

Foundry Prototyping Services

Flexible Manufacturing options

- Full Mask Set
  - Full flexibility in timing and volume
  - Reasonable NRE* cost
- MLM (Multi Layer Mask)
  - Full flexibility in timing for small volume production
  - Significantly reduced NRE costs
- MPW (Multi Project Wafer)
  - Ideal solution for prototyping and low volume production
  - Lowest NRE costs





* NRE = Not Recurring Engineering

Probe & Analytics Service

Probe Area

In House electrical testing enable fast feedback about the quality and yield of products

- 7 Days/week, 24h shift coverage
- PCM (Process control monitor)
- Memory Tester (DRAM/SRAM)
- Mixed Signal Tester
- Imager testing

Chemical Laboratory (Incoming Quality)

Provide analytical and material competences to meet products and operations requirements.

Failure Analysis Lab

Full equipped Laboratory for internal and external Failure Analysis

- 7 Days/week, 08-20 shift coverage

Focus Ion Beams
2 x Dual Beam FEI Strata 235

Scanning Electron Microscopes
2 x Hitachi 4700
1 x Hitachi 4800 (with EDX)
2 x FEI Nova-600 Nanosem

TEM/STEM:
TECNAI G2 F30 S-Twin equipped with Lorentz Lens, Bi-prism. EELS and EDX detector. Holography, Tomography

Wafer Level Reliability Equipment

... more services available

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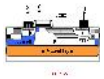
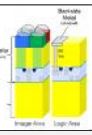
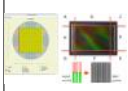
Technology Platform (FOT) Summary

150nm Technology Node
Modular Platform

LF15A		
1.8V, 3,3V, 5.0V		
1P7M		
 MIM	 LDMOS*	 RF
1fF, 2fF	**36V**	**Inductors/ Varactors**
PDK 1.0.0 MP		

110nm Technology Node
CIS Platform

LF11IS		
1.2V, 3.3V		
1P6M		
		
2.4um Reference Pixel	**BSI**	**Stitching**
PDK 0.8.0 PT		

PDK Readiness
PT=ProtoType
MP=Mass Production

Power Market - 150nm Platform and COT

LED, AC2DC

IGBT
up to 700V

Motor driver, POE*
(*Power over Ethernet)

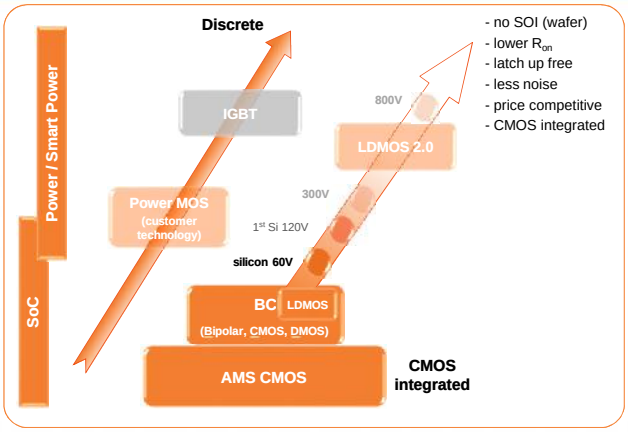
up to 80V, low R_{on}

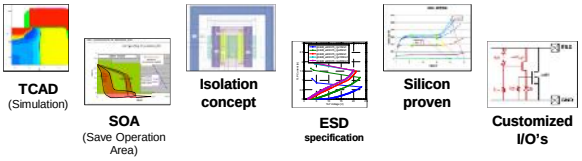
PMIC, digital Power

Vg=3.3V / 5V
up to 80V

Audio, Analog, RF

Vg=3.3V
full isolation





… offer a full solution based on the specifications of the customer, including SOA, ESD and I/O's.

LF15A Brief Introduction

Automotive qualified
Grade "0"
-40°C till 150°C

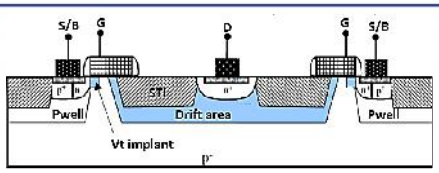
Aerospace qualification ongoing

LF15A

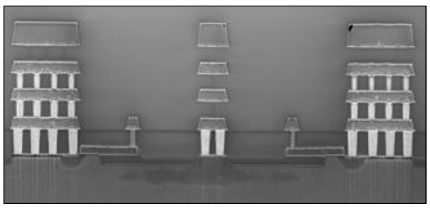
Process	Libraries	EDA
1 Poly	GPIO library 3.3V, 1.8V and 5V	Analog Mixed Signal iPDK for Cadence Virtuoso 6.1.x
4 – 6 Metal (330nm, 800nm Alu)	RF-Library	Analog Mixed Signal iPDK for the IPL-Alliance
extra Thick Top Metal (6µm Al)	Digital Library 1.8V low leak, high speed >400 cells, 137*kGates/mm² good rad hardness values	Memories
2 level of deep NWell	chip finishing	SRAM
gate oxide thickness 2.8 / 6.8 / 16.0 [nm]	Design Rules	OTP
shallow trench isolation (STI)	Physical Gate L: 150nm Contact/Via size: 180/240nm Metal pitch: 480nm	EEPROM (single poly)
intermetaldielectric: TEOS		
cobalt salicidation		

* GateDensity = (1 / NCS) * 1000 [kGates/mm²]
NCS = 4 x (TA / TTC) [µm²]
TA = The entire area of all standardcells (without physical cells).
TTC = The number of all MOS in all cells (without physical cells).
4 x : Multiplier used to get NAND2 equivalent.

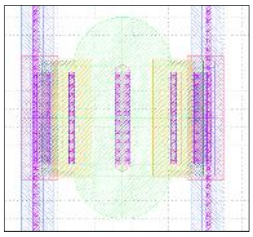
40V Automotive LDMOS Specification



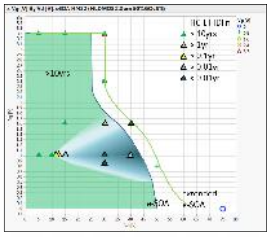
schematic X-section of a HV-NLDMOS transistor



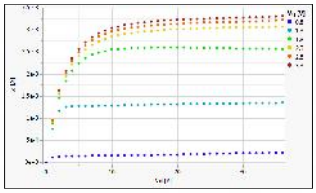
X-section example of a HV-NLDMOS transistor



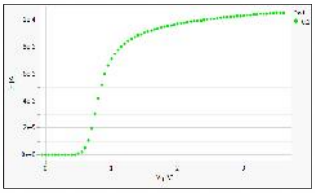
simplified top view of the HV-NLDMOS transistor with most relevant layers up to the first metal



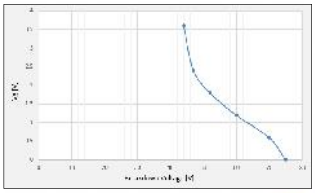
HC-SOA for Idlin degradation



Id-Vd characteristic for different Vg at 30° C (for a device with W=10µm)



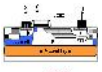
Id-Vg characteristic linear operation (Vd = 0.1V) at 30° C (for a device with W=10µ)



Breakdown voltage as a function of Vg

Technology Platform (FOT) Summary

150nm Technology Node Modular Platform

LF15A		
1.8V, 3,3V, 5.0V		
1P7M		
 MIM	 LDMOS*	 RF
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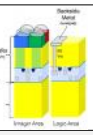
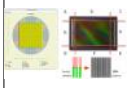
110nm Technology Node CIS Platform

LF11IS		
1.2V, 3.3V		
1P6M		
		
2.4um Reference Pixel	**BSI**	**Stitching**
PDK 0.8.0 PT		

PDK Readiness
PT=ProtoType
MP=Mass Production

Imager Go-To-Market Strategy

Visible Light

- Automotive
- Industrial / Machine Vision
- Medical
- High Speed
- Mobile
- DSLR

Infrared

X-ray

- Use imaging technology & application knowhow to service full range of optical sensing: analog PDs …CIS ... to high-end 3D

Photo Diode Sensors

stand alone
process
discrete
photo diode

Standard CIS
CMOS Image Sensors

FSI (incl. light pipes)
Global shutter
BSI

Highend CIS
CMOS Image Sensors

Photo Detectors, SiPM

Silicon Photo Multiplier
e.g. particle accelerator
detector magnetic
Resonance
tomography

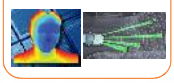
SiPM with
e.g stacked
CMOS

SiPM/Sensor-ASIC Integration

Single Photo Avalanche Detector
Integrated inside CMOS

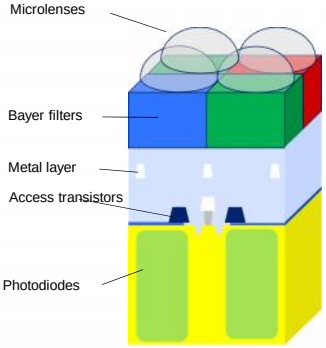
CMOS-SPAD

3D Imaging
Time of Flight
SPAD

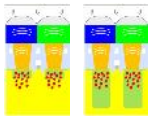


HEP
(high energy physic)

CMOS Image Sensors - FSI Capabilities



Deep Photo Diode

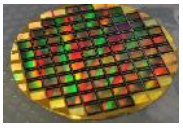


Max implant energy capability:
- Boron 2800 keV
- Phosphorous 4800 keV

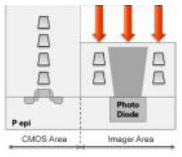
Implant masking approach:
- Resist up to 15:1 Aspect Ratio
- Hard mask

Isolation Implants

Customized Wafer Type

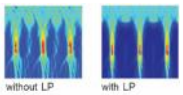


Metal Recess

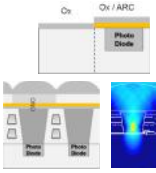


Light Pipes and Optical Stack Optimization

High refractive index Polymer (n = 1.6-1.7)

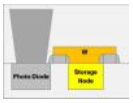


ARC & stack formation



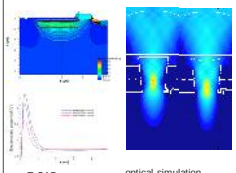
Modules for Global Shutter

Buried Tungsten Light Shield

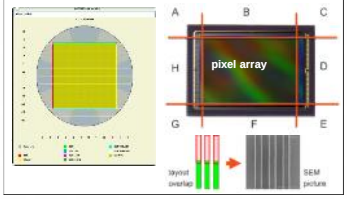


Metal ARC

Pixel Simulation Service



Stitching (customer / design specific development)

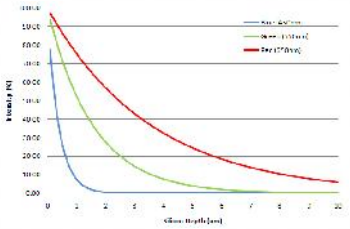


Example of Customized Process Module

Photo Diode Forming Implants

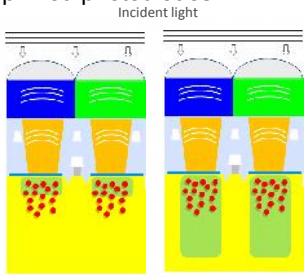
Motivation:

- More collected electrons



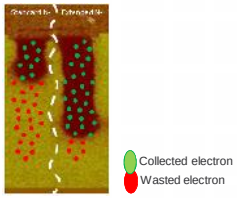
Key process steps:

- Implants to form customized PDs
- Deep implant scheme to fabricate pinned photodiodes

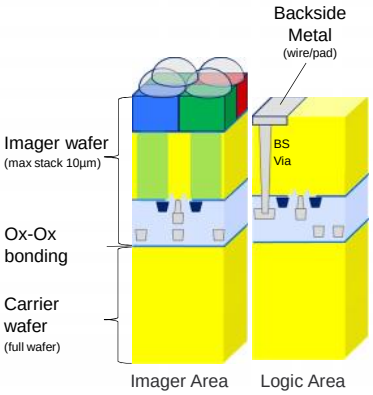


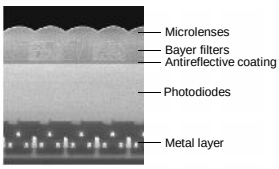
Enablers:

- High energy ion implantation capability
- High aspect ratio resist
- Hard mask

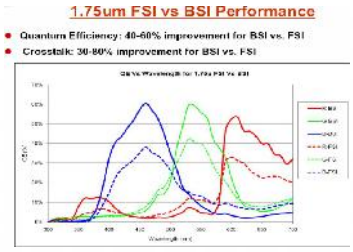


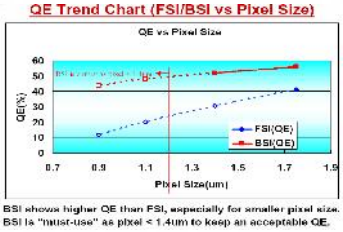
CMOS Image Sensors - BSI Capabilities





100% fill factor, with reduced stack height decreasing crosstalk and improving sensor angular response.

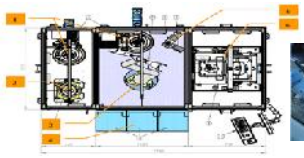


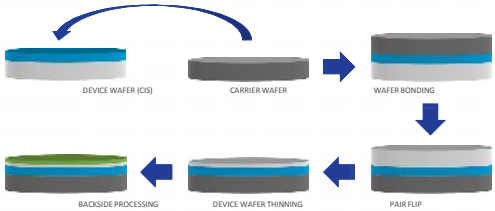


CMOS Image Sensors: BSI Enablers

Fusion Bonding

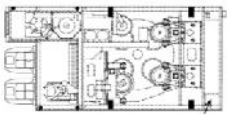
1) Cleaning module
2) Plasma Module
3) Robot
4) Load Port
5) Optical Pre-aligner
6) Smart View aligner

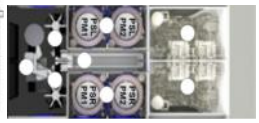




Si Grinder and Si Wet Etch

- Post grinder Silicon thickness: 20-30um (TTV < 3 um)
- Final Silicon Thickness: 2-4um (3 sigma < 0.2um)





Laser Anneal

- l = 308nm;
- Pulse duration = 160-180ns;
- Melting depth at 2J/cm2 = 70nm
- 95% of thermal budget is limited to 3 µm
- Single Wafer process
- Max size of laser beam on stage 20mm x 20mm

LF11IS – 110nm CIS Technology Platform

Voltage domains

- 1.2V digital (logic and SRAM)
- 3.3V analog and pixel

Process notes

- Shallow Trench Isolation (STI); Design Rules: 0.13µm/0.13µm L/S array (0.15µm/0.15µm pery)
- Retrograde channel doping by high-energy implants;
- 2-Gox (22Å for 1.2V; 70Å for 3.3V);
- Gate Poly line width: Design Rules: 0.11µm/0.15µm L/S
- L-Spacer
- Co Salicide w/ Ox/Nit Sa-Block and Ti cap;
- Contacts made with Tungsten; Design Rules: 0.14µm
- MIM capacitors;
- 4 - 6 Al Metal Layers;
- Tungsten Vias; Design Rules: 0.15µm Via1; 0.19µm Via X
- Four 193nm ArF Photo levels (Diff, Poly, CT, M1)
- BSI

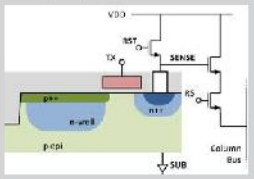
Design Rules

- LF11A for analog, logic and SRAM
- Dedicated Pixel DRs

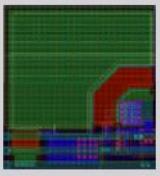
LF11IS CIS PDK Content

Standard

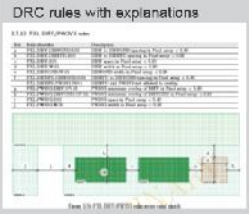
- Example pixel x-section



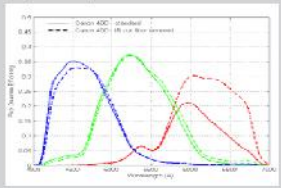
- Example pixel gds



- Pixel layout rules
  DRC rules with explanations

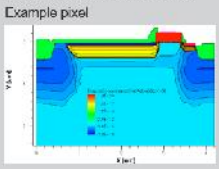


- base performance data of ref. pixel
  (QE,DC,...)



Add on*

T CAD simulation results of the Example pixel

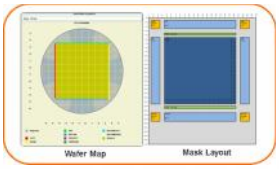


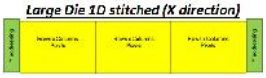
*release only for dedicated customers after special IBL/LLD approval

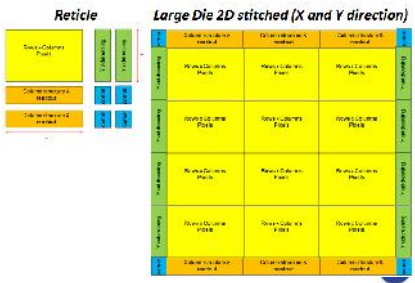
- "LF11IS" PDK for Automotive Grade 1 designs
- Special PDK setup & support for high performance products thru dedicated pixel setup flow, integrated process modules, …

Stitching Capability

- Need for image sensor sensors with larger size than the field of a semiconductor lithography equipment is not new
- However the challenge is the need of customized solutions for the wide field of different applications i.e.
  - 1D Stitching in low complexity (non CMOS) optical sensors (PDs) for large panels and thus interaction with final assembly concepts – in production at LF
  - 2D Stitching within wafer with high complex circuitry and thus challenge of device/layout optimization on stitching borders – in development at LF



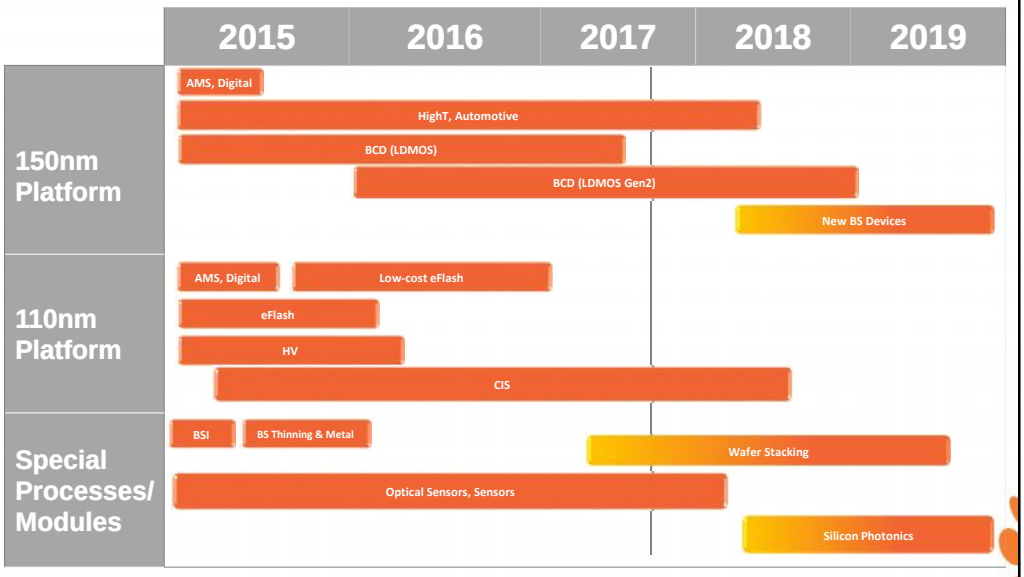




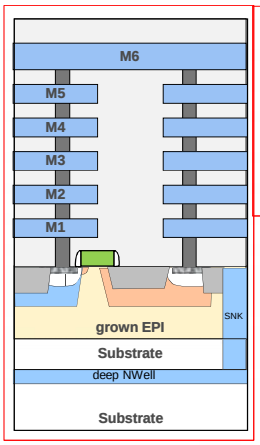
Outline

- The Avezzano Fab
- The Technology Opportunities
- **The Development Perspective**

Perspective Technology Roadmap

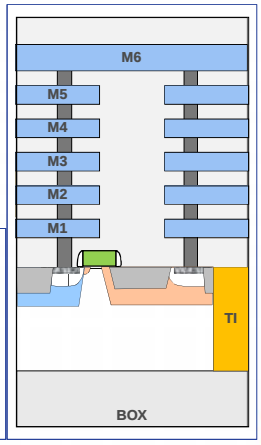


BCD Available Alternatives: EPI or SOI



Junction-isolated p-LDMOS with EPI process
Lateral Isolation: Implant Sinkers
Vertical Isolation: Implant Deep NWell
Pros
improved BV
Cons
poor integration of multi-voltage domains, Expensive

p-LDMOS with SOI technology
Lateral Isolation: Deep Trenches
Vertical Isolation: Buried Oxide
Pros
improved BV, integration of multi-voltage domains, low substrate noise, latch-up free
Cons
Very Expensive

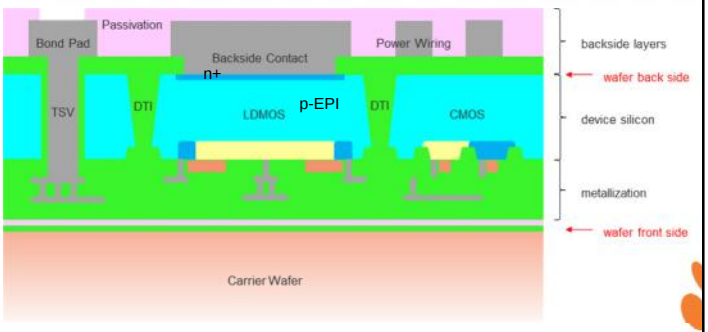


BackSide p-LDMOS

Another alternative

- developed a novel BCD technology which offers all advantages of SOI technology but with lower manufacturing cost: the substrate is to a large extent removed and the devices are completed by manufacturing processes performed on the thinned wafer backside (LFoundry patent)

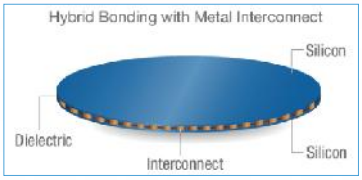
Schematic of novel BCD technology using wafer backside processing

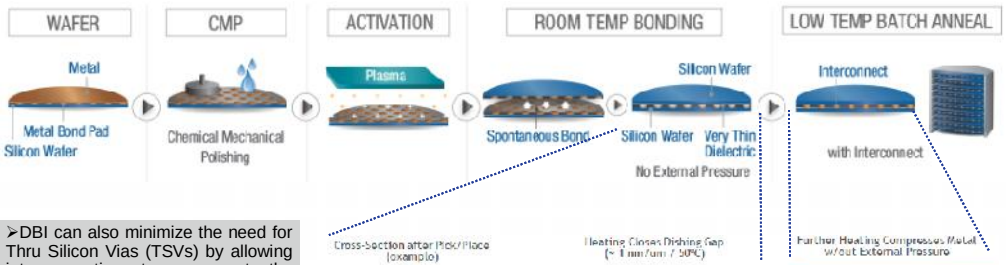


Same benefits of the SOI approach, more cost effective

Hybrid Wafer Bonding Technology

➢DBI® is a low temperature hybrid direct bonding technology that allows wafers to be bonded with exceptionally fine pitch 3D electrical interconnect.
➢Alignment and bonding is performed at room temperature.
➢It leverages industry-standard wafer bonding equipment, enabling the high-throughput, low cost-of-ownership fabrication process required for high volume market applications.

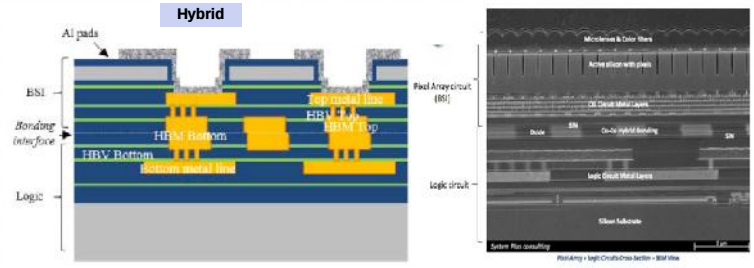




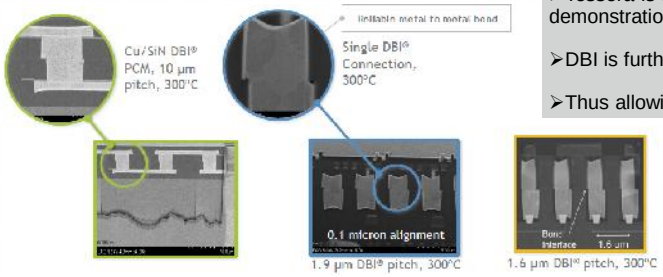
➢DBI can also minimize the need for Thru Silicon Vias (TSVs) by allowing interconnection to occur at the bonding surface, improving electrical performance.
➢By incorporating dielectric bonding, it eliminates the need for under-fill while providing excellent thermal performance, reliability and hermeticity.

Source: Experi

Hybrid Wafer Bonding Technology



Source: System Plus



➢Tessera is capable of 1.6µm pitch in demonstration vehicles.

➢DBI is further scalable to <1µm pitch

➢Thus allowing within pixel interconnect

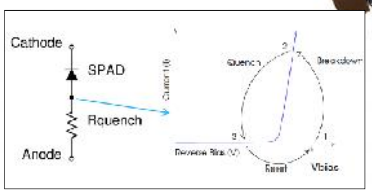
Source: Xperi Tessera

SiPM (Silicon PhotoMultipliers)

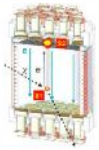
Thanks to its high efficiency and low noise, SiPM are replacing PhotoMultiplier Tubes (PMT) in various applications

Commercial: PET

(Positron Emission Tomography)



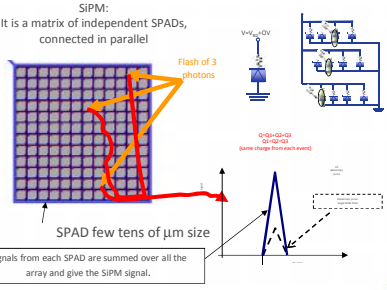
Big Science:



Detection of weak scintillation signals from nuclear recoils produced in elastic collision of WIMPs with ordinary matter.

Observation of Cosmic Gamma-Rays by means of Cherenkov radiation detection.

SiPM:
It is a matrix of independent SPADs, connected in parallel



Signals from each SPAD are summed over all the array and give the SiPM signal.

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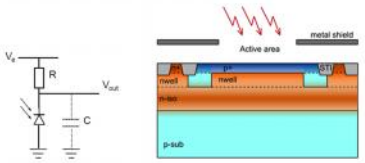
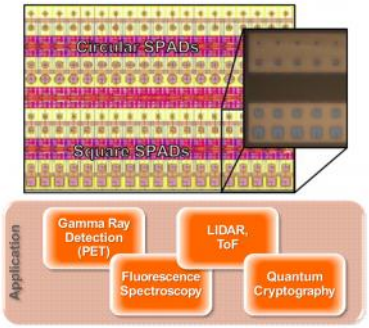
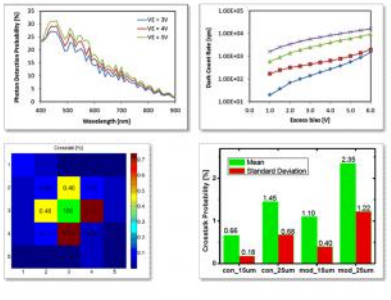
SPAD Devices to Enable ADAS with ToF Sensing

- Several SPAD structure development in Avezzzano fab (150&110nm CMOS platform)
- Circular and Square SPADs, from 5um to 20um
- Complete performance characterization
- Good breakdown voltage uniformity (40mV)
- Small crosstalk (1%-2.5%)







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Technology for the Local Network

Opportunity to create a positive interactions among the local microelectronic elements and expertise (product company, design house, foundry, research center, university, institution, etc..)

Few examples:

- Technology exploitation
  - ✓ Space application → 150nm platform for ESA project
- Technology transfer
  - ✓ Science application → SiPM for different application
- Technology development
  - ✓ Improved sensor → INFN SEED project
- Technology sharing
  - ✓ Physical characterization techniques → Open Lab project

Summary

- LFoundry is an Italian 8" silicon fab, evolved form the IDM to foundry business model, specialized in:
  - Optical Sensors (CIS, Discrete PD, SPAD, SiPM)
  - Analog and Mixed Signal
  - Smart Power (LDMOS)
- Other than manufacturing services, LFoundry is open to innovative solutions through Joint Development Programs, open also to scientific collaborations.
  - Open to partnerships with RTOs, SMEs and Universities.
- Interest in increasing the technology portfolio in the Optoelectronics and in entering into new technology line, like e.g. Silicon Photonics.


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for great visions
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sergio.dalberto@lfoundry.com
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